WHAT IS CLAIMED IS:

1. A hybrid semiconductor device, comprising:

   a first portion being relatively resistant to breakdown; and

   a second portion being less resistant to breakdown.

2. The device of claim 1, wherein the first portion comprises a MOSFET transistor device.

3. The device of claim 1, wherein the second portion comprises a diode.

4. The device of claim 1, wherein the first portion comprises a MOS transistor and the second portion comprises a diode.

5. The device of claim 3, where the diode has the identical structure as the MOS transistor, except for a source region.

6. The device of claim 1, where breakdown occurs at a higher voltage in the first portion, and at a lower voltage in the second portion.

7. The device of claim 6, where the breakdown voltage differential is due to a difference in field plate length.

8. The device of claim 7, where the transistor is an SOI- LDMOS device.

9. The device of claim 8, where the transistor is any of an NMOS or PMOS device.

10. A method of constructing a rugged transistor device, comprising:

integrating in the device one or more nontransistor regions whose future performance is not damaged by an overvoltage breakdown; and

arranging the device such that overvoltage breakdown always occurs in said nontransistor region.

11. The method of claim 11, where the nontransistor regions each comprises a diode;

12. The method of claim 12, where the nontransistor regions have a lower breakdown voltage than that of the transistor.

13. The method of claim 13, where the nontransistor regions have a shorter field plate length than that of the transistor.

14. The method of claim 14 where the diode regions have a nearly identical structure as the transistor regions.

15. A hybrid lateral thin-film Silicon-on-Insulator device comprising:

a first region comprising:

a semiconductor substrate, a buried insulating layer on said substrate, and a lateral MOS device in an SOI layer on said buried insulating layer and having a source region of a first conductivity type formed in a body region of a second conductivity type opposite to that of the first, a lateral drift region of said first conductivity type adjacent to said body region, a drain region of said first conductivity type and laterally spaced apart from said body region by said lateral drift region, a gate electrode over a part of said body region and over a first part of said lateral drift region adjacent to said body region, said gate electrode being insulated from said body region and drift region by a first insulation region, with a field plate comprised of conducting material extending laterally over said lateral drift region and being electrically connected to said gate electrode; and

one or more second regions integrated with the first region, said second regions being identical to the first region, except not comprising said source region, and having a field plate of shorter length than that of the first region.

16. The device of claim 15, where the width of each of the second regions is at least as long as the lateral drift region.

17. A method of obviating bipolar second breakdown in MOS transistor devices, comprising:

integrating one or more diode regions in the MOS device; and

setting the breakdown voltage of the diode devices to be lower than that of the MOS transistor regions.

18. The method of claim 17, where the lower breakdown voltage of the diode regions is set by shortening the field plate relative to the transistor regions.